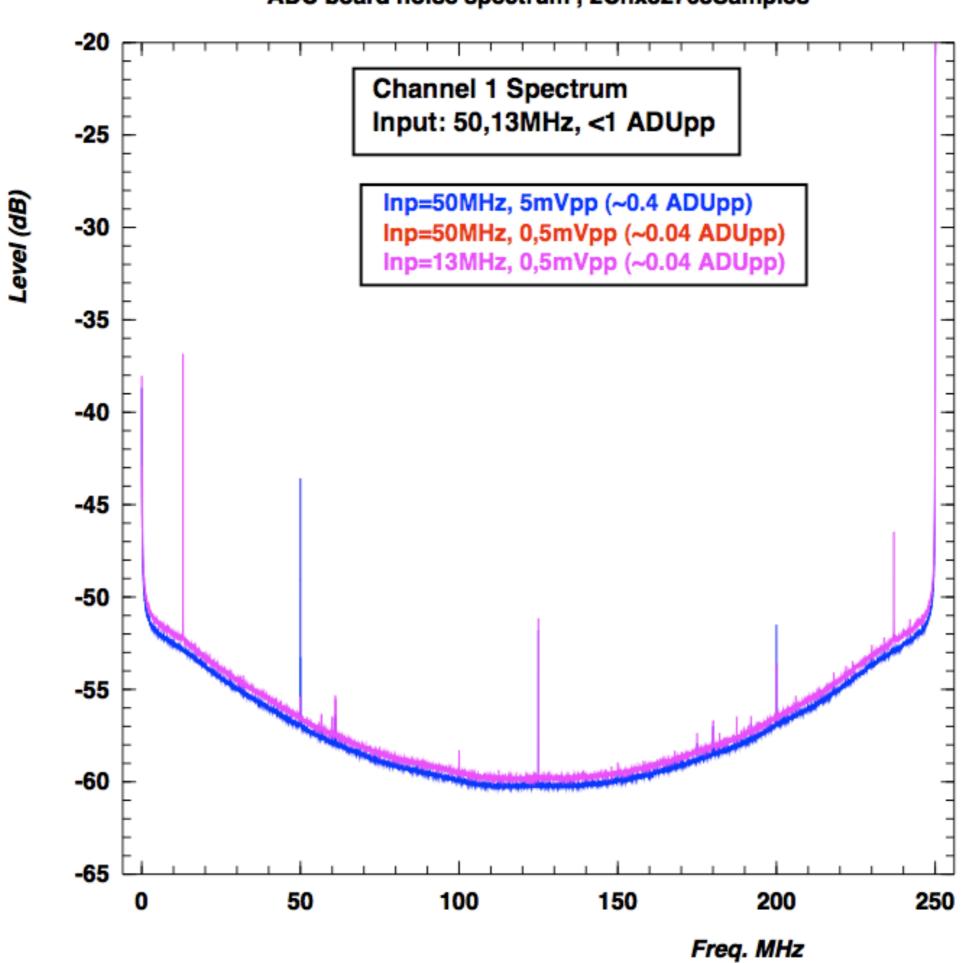
H2I/CRT electronic: Plans

CRT meeting - 09 April 2009

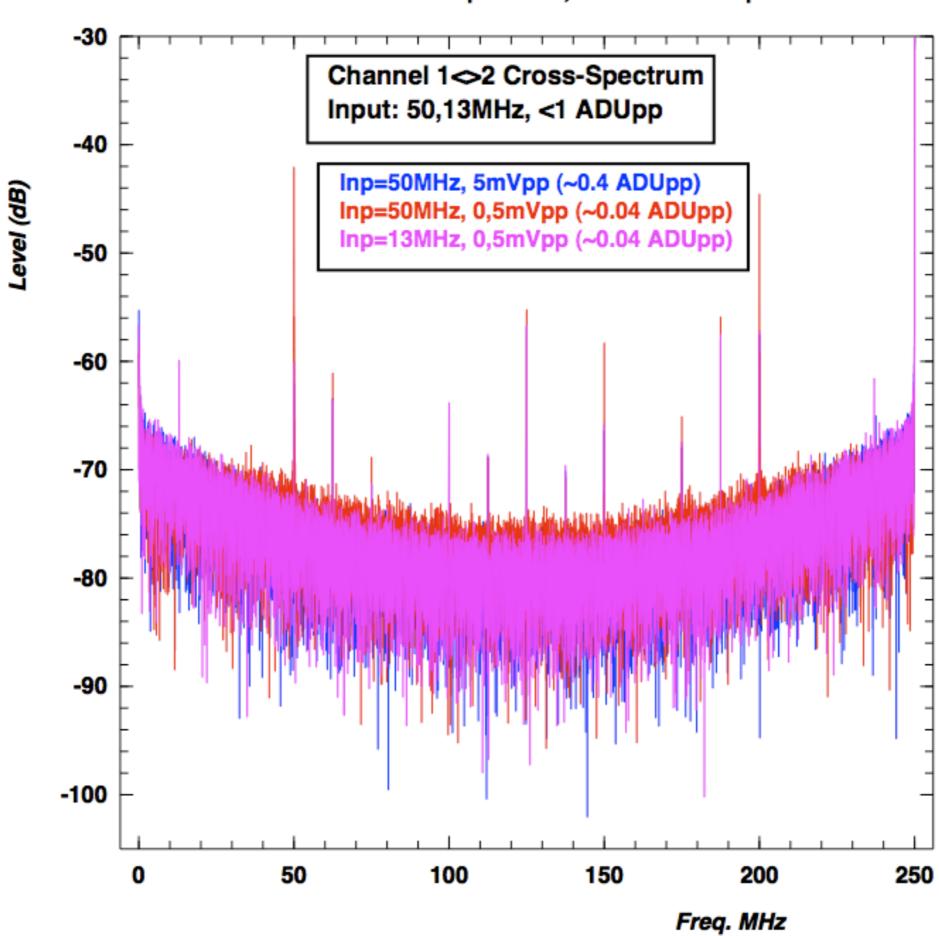
R.Ansari, on behalf of Saclay-Orsay 21cm BAO team

- DFS (ADC) board noise performance
- Future test plans (Pittsbutgh, ...)
- Long term development issues

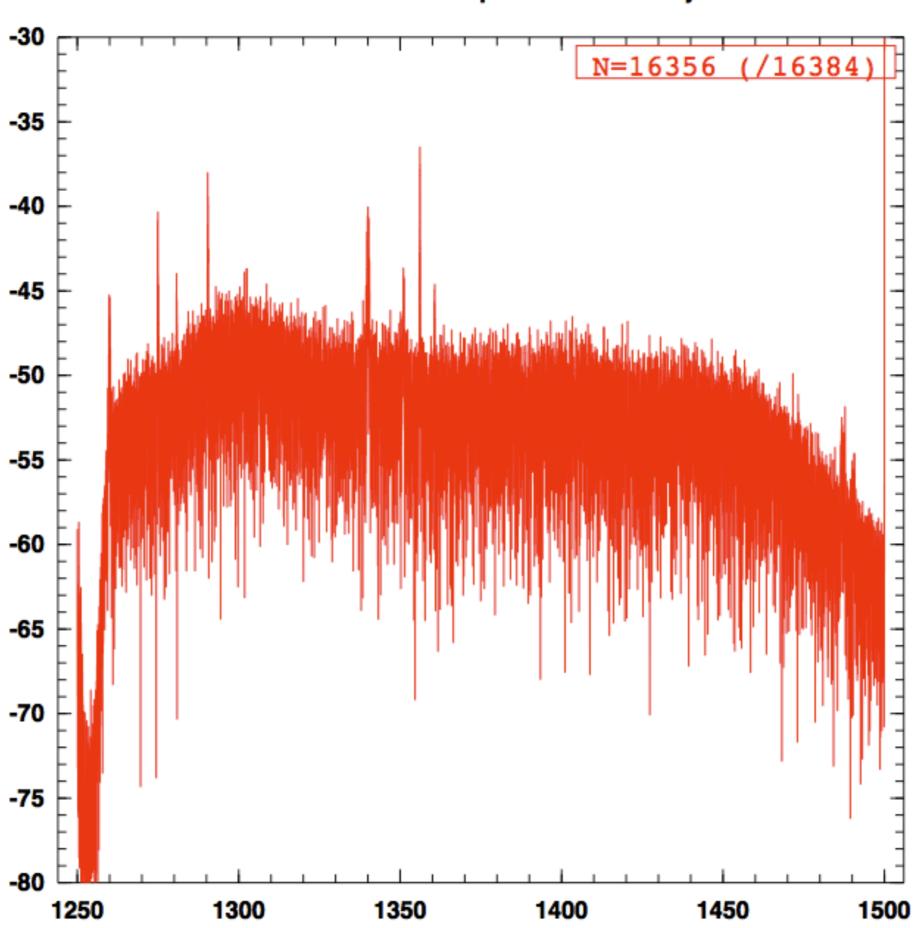
ADC board noise spectrum, 2Chx32768Samples



ADC board noise spectrum, 2Chx32768Samples



2Chx32768 CrossSpectrum At Nancay



Firmwares

- DFS/ADC board firmware: RawData, FFT8K+8K
 - Some improvements needed for increasing reliability
- Current version (v=49.4): 64 kB maximum packet size, SGDMA with ~ 500 MB/s DMA transfer rate to memory, ~ 200 MB/s maximum sustained acquisition rate on - Handles the byte-swap
- Dual fibre read-out firmware under development

Tests at Pittsburgh (I)

- Aim: Multi-channel acquisition + beam reconstruction
- We need to define a detailed test program :
 - Number of channels, I or two cylinders
 - Some calibration procedure
 - The acquisition configuration (hardware/software)
- The processing software should be prepared according to the defined program

Tests at Pittsburgh (2)

- Logistic issues : define possible dates
- A number of simple questions has to be answered :
 - cable types and length
 - Length of optical fibres (we need to order them)
 - The operation can be made simpler if we can avoid to transport the computers (PC's with PCI-Express 4X + (RAID) disks)
 - If yes, we will have to ship one PCI-Express card to be tested on the computer

Electronic card manufacturing schedule (1)

- DFS/ADC board 4 channel/board We are currently using the two initial prototype boards (v=1). (2)
- A third board based on the existing first PCB version is being manufactured (+| End of April/May)
- Two new version of the PCB (V1.2) is being manufactured
- The two new boards should be at LAL in June (+2 June / before summer)
- If OK, 5-6 additional boards will be fabricated (+6)
- We should have a total of 10 boards (40 channels) in summer or september 2009